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Optimizing DSP-Based Digital Filtering Systems With Application-Specific FIFOs

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First-In, First-Out Technology

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November 1994

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Contents

Introduction

The new Texas Instruments (TI) SN74ACT36xx 36-bit clocked FIFO family is designed to interface to 32-bit floating-point digital signal processors (DSPs), such as TI's leadership TMS320C3x and TMS320C4x families of DSPs. These FIFOs can significantly improve system throughput by permitting DSPs to run optimally, while allowing for high-integrity data transfer. With depths ranging from 256 to 1024 words in unidirectional and bidirectional formats, and features such as synchronous retransmit and mailbox-bypass registers, the DSP application FIFOs enhance the broad spectrum of FIFOs available from TI.

This application report includes two examples of the use of DSP application-specific FIFOs in optimizing DSP-based digital filtering systems. Digital filters such as the finite-length impulse response (FIR) filter are typically used in image- or voice-processing applications. In each example presented below, the patented synchronous-retransmit FIFO feature is used with a DSP for FIR digital filtering. Descriptions of patented synchronous retransmit and digital filtering are followed by the two applications. The TMS320C31 and TMS320C40 floating-point DSPs and the SN74ACT3641 (1024 × 36) unidirectional and SN74ACT3638 (512 × 32 × 2) bidirectional clocked FIFOs are used to illustrate the discussion.

Patented Synchronous Retransmit

The synchronous-retransmit feature of the SN74ACT3638 FIFO allows data stored within the device to be reread starting at a user-selected position. Conventional retransmit, by way of comparison, only permits rereads from location zero in the FIFO. The 512 x 32 dual port SRAM that buffers data from port A to port B on board the SN74ACT3638 die can be programmed for retransmit. Placing the device in the retransmit mode selects a beginning word and prevents ongoing write operations from destroying the retransmit data. Data vectors with a minimum length of three words can be reread repeatedly, starting at the selected word. The FIFO can be taken out of the retransmit mode at any time, allowing normal operation to resume. The operation of synchronous retransmit is similar for the SN74ACT3641. The primary difference is the size of the SRAM.

Digital Filtering

Many DSP-based systems require filtering. The FIR or delay filter is one type of digital filter that is commonly implemented in such applications. The FIR filter in the time domain takes the general form of:

$$y(n) = \sum_{i=0}^{N-1} h(i) \times x(n - i)$$

Where:

where *y(n)* is the output sample at time *n*, *h(i)* is the *i*th coefficient or impulse response, and *x(n–i)* is the *(n–i)*th input sample.

The FIR filter, as described by this equation, and the synchronous-retransmit feature of the DSP application FIFOs form the basis of the filtering examples described on the next page.

Digital-Image Filtering With the TMS320C31

DSPs such as the TMS320C31 can perform mathematically-intensive algorithms in real time. The FIR filter described by the earlier equation is such an algorithm. To generate *y(n)*, *N* multiplications and additions must be performed. The product of sums computation is very demanding, particularly in the instance where *N* is large. Real-time digital signal processing requires that there is no user-discernable delay in a given process. As mentioned above, DSP-based FIR filtering is often the principal component of image-processing applications. In this case, the DSP is required to complete its real-time processing within a given frame update. If the process is not completed in this period, aberrations in the final image, such as flicker, are likely to be detected by the observer.

The capability for parallel multiply/add operations and circular addressing permits easy implementation of this FIR filter with the TMS320C31 DSP. The parallel multiply/add operation allows a multiplication and addition operation to execute in one machine cycle, and the circular addressing generates a finite buffer of length *N* for the data *x(n)*.

The SN74ACT3638 is easily interfaced to the TMS320C31 (Figure 1) to provide buffering and storage of the FIR filter coefficients, *h(i)*. The SN74ACT3638 is chosen for several reasons. The width of the FIFO matches that of the DSP (32 bit). The FIFO also has bidirectional capability allowing for data flow from FIFO to DSP and vice versa, and the FIFO has the retransmit feature required for this application. Utilized for coefficient storage, the FIFO serves as a zero-wait-state SRAM. By using the FIFO retransmit feature (Figure 2), the filter coefficients are efficiently transferred to the DSP on an as-required basis. This design provides significant savings in terms of complexity, cost, space requirements, and overall chip count when compared with other methods such as storing the coefficients in either an external SRAM or an EPROM. Using the DSP internal RAM to store the coefficients causes delay in transferring the coefficients from the buffering FIFO to RAM. This overhead penalty and inefficient use of RAM is eliminated by using the synchronous-retransmit feature of the DSP application FIFO.

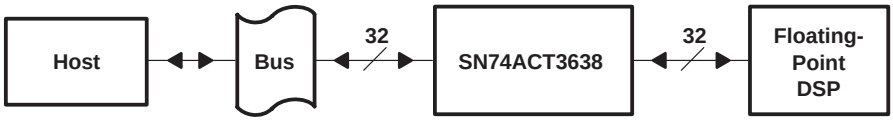

Figure 1. Bidirectional FIFO Interface for FIR Filtering

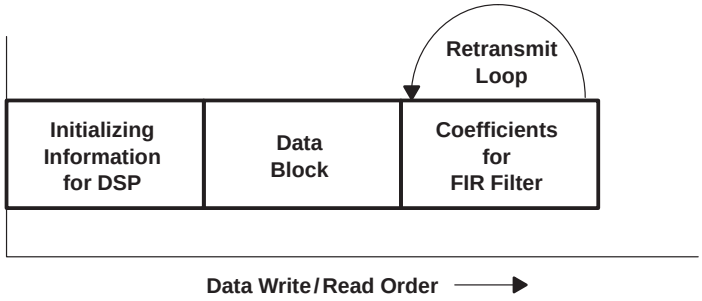

Figure 2. Using a FIFO for Coefficient Storage in FIR Filtering

Two external input/output (I/O) flags (XF0 and XF1) of the TMS320C31 are configurable as inputs or outputs under software control. For digital FIR filtering, the I/O flags are used to control the retransmit function of the FIFO, providing a programmable and seamless DSP interface.

Digital-Voice Filtering With the TMS320C40

Speech-recognition systems are another example of digital-processing applications that use FIR filtering techniques. Like the image-processing systems mentioned previously, speech recognition also requires real-time operation. Obvious delays between spoken and recognized words are unacceptable for the system to be considered real-time. Figure 3 shows the essential components of a speech-recognition system that implements FIR filtering. The components of this system are a TMS320C40 DSP, a multiply-accumulate (MAC) block, and two FIFOs. The filtering function is described by the earlier equation. In this design, the TMS320C40 DSP is used to generate a series of coefficients or weighting factors that are used by the FIR filter. The SN74ACT3641 FIFO is interfaced directly to the DSP. This FIFO is chosen for its wide width, high speed (up to 67 MHz), and synchronous-retransmit feature. The fine-pitch packaging option, known as the thermally enhanced thin quad flatpack (TQFP) package, also permits significant space savings for this single-chip FIFO solution. Similar to the first example, the FIFO is used to store the filter coefficients, *h(i)*. The synchronous-retransmit capability is used to transfer the coefficients to the MAC, as required. A second FIFO is needed to provide rate matching between the incoming input samples, *x(n–i)*, and the MAC. The input samples are the digitized results of a transducer or analog to digital (A/D) converter. The data, in this case, is voice information.

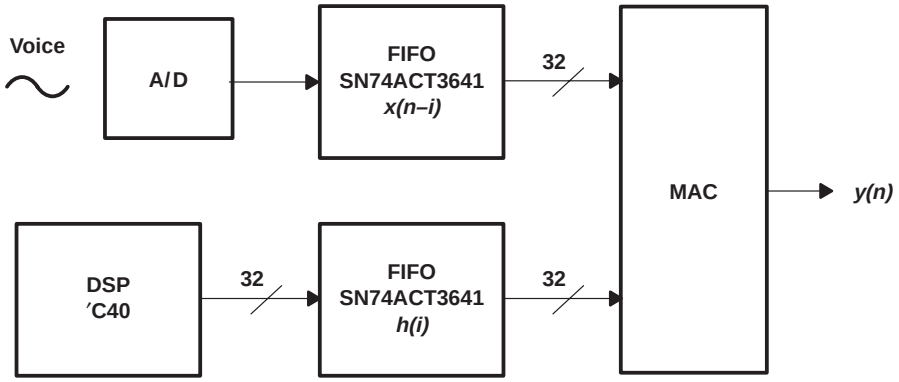

Figure 3. Speech Recognition FIR Filter

This implementation of a one-dimensional FIR filter can be easily reconfigured to a two-dimensional filter by adding a third FIFO in series with the FIFO that provides rate matching between the A/D converter and the MAC. The result is a multistage delay FIR filter that is capable of handling two-dimensional data such as that generated by raster scanning an image in both the *x* and *y* directions.

Conclusion

As illustrated by the image- and voice-processing examples presented in this application report, TI's DSP application FIFOs provide a seamless interface to DSPs such as the TMS320C31 and TMS320C40. The advantages of high-speed performance, small packaging options, and wide bus widths, combined with a powerful feature set, permit optimum solutions to be realized with these FIFOs. Although digital FIR filtering is just one example, there is a vast array of other applications in which FIFOs can be used to optimize the performance of DSP-based systems.