Medium-Pin-Count Surface-Mount Package Information

First-In, First-Out (FIFO) Technology

SSPA001B
February 1997

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Introduction

Texas Instruments (TI) provides ten types of plastic surface-mount packages for CMOS FIFO memory devices. These packages and the data bus width that each package supports are listed in Table 1.

Table 1. Plastic Surface-Mount FIFO Packages

PACKAGE	NO. OF DATA BITS
24-pin SOIC (DW)	1
28-pin SOIC (DW)	1
44-pin PLCC (FN)	9
64-pin TQFP (PM or PAG)	9
56-pin SSOP (DL)	18
68-pin PLCC (FN)	18
80-pin TQFP (PN)	18
80-pin PQFP (PH)	18
120-pin TQFP (PCB)	32 or 36
132-pin PQFP (PQ)	32 or 36

PLCC = plastic leaded chip carrier
PQFP = plastic quad flat package
SOIC = small-outline integraged circuit
SSOP = shrink small-outline package
TQFP = thin quad flat package
(xx) = TI package nomenclature

This application report discusses several topics concerning the FIFO packages listed in Table 1:

- Thermal impedance, Θ_{JA}, and the chip junction temperature of the device
- The need for dry packing to maintain safe moisture levels inside the package
- Three kinds of packing used by TI to ship FIFOs to customers
- Package dimensions, including two-dimensional drawings that show areas, heights, and lead pitches
- Area comparison of surface-mount packages used for commercial FIFO memories
- Test sockets available for surface-mount FIFO packages

Thermal Impedance

Thermal impedance is defined as the ability of a package to dissipate heat generated by an electronic device and is abbreviated as Θ_{JA}. Θ_{JA} is the thermal impedance from the integrated-circuit chip junction to the free air (ambient). By far the most common measure of package thermal performance is Θ_{JA}. Θ_{JA} values are also subject to interpretation. Factors that can greatly influence the measurement and calculation of Θ_{JA} are:

- Board mounted (yes or no)
- Traces (size, composition, thickness, and geometry)
- Orientation (horizontal or vertical)
- Ambient (volume)
- Proximity (any other surfaces near the device being measured)

In August 1996, the Electronics Industries Association released Standard EIA/JESD51-3, “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.” This standard provides guidelines for designing the test board used in taking thermal-impedance measurements of integrated-circuit packages. Prior to the release of this standard, thermal-impedance data for similar packages varied greatly across the industry because of the use of different test-board designs. In particular, the characteristics of the test board were found to have a dramatic impact on the measured Θ_{JA}. As the industry converts to this standard test-board design, the variation in thermal characteristics data caused by the board should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimension: 3.0 in. × 4.5 in. for packages < 27.0 mm in length
- Board dimension: 4.0 in. × 4.5 in. for packages > 27.0 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 0.984 in. (25.0 mm)

TI’s Standard Linear and Logic (SLL) product group uses EIA/JESD51-3 to design the test boards for thermal-impedance measurements. The parameters outlined in this standard are used to set up thermal models.

The unit for Θ_{JA} is degrees Celsius per watt. Table 2 lists Θ_{JA} for SOIC, SSOP, PLCC, TQFP, and PQFP packages under four different air-flow environments: 0, 150, 250, and 500 linear feet/minute. The chip junction temperature (T_J) can be determined using equation 1.

$$T_J = \theta_{JA} \times P_T + T_A \tag{1}$$

Where:

T_J = chip junction temperature (°C)
Θ_{JA} = thermal resistance, junction to free-air (°C/watt)
P_T = total power dissipation of the device (watts)
T_A = free-air (ambient) temperature in the particular environment in which the device is operating (°C)

Table 2. Thermal Impedance, Θ_{JA}, for FIFO Packages

PACKAGE†	LEAD FRAME	Θ_{JA} (°C/W)				ACTUAL/ MODEL
		0 LFPM	150 LFPM	250 LFPM	500 LFPM	
24-pin SOIC (DW)	Copper	80.7	53.7	47.5	40.7	Model
28-pin SOIC (DW)	Copper	78.2	54.3	48.4	41.9	Model
44-pin PLCC (FN)	Copper	46.2	38.6	35.4	31.6	Model
56-pin SSOP (DL)	Copper	73.5	62.3	59	54.6	Actual
64-pin TQFP (PM)	Copper	66.9	53.6	47.6	40.6	Model
64-pin TQFP (PAG)	Copper	58.2	48.8	45.2	40.3	Actual
68-pin PLCC (FN)	Copper	39.3	33	30.5	27.6	Model
80-pin TQFP (PN)	Copper	61.5	52.8	49.3	44.6	Actual
80-pin PQFP (PH)	Alloy 42	76.1	67.9	61.4	53.6	Model
120-pin TQFP‡ (PLB)	Copper	28.1	22.3	21	18	Model
132-pin PQFP (PQ)	Copper	38.8	27.3	25.1	22.4	Model

† (xx) = TI package nomenclature
‡ Heat slug molded inside the package

Θ_{JA} generally increases with decreasing package size, but this is not true with the 120-pin SQFP package. A heat slug molded inside the package absorbs a large amount of heat dissipated by the device. As a result, this package provides a relatively low Θ_{JA} (as low as 18°C/W at 500 LFPM air flow).

Package Moisture Sensitivity

When a plastic surface-mount package is exposed to temperatures typical of furnace reflow, infrared (IR) soldering, or wave soldering (215°C or higher), the moisture absorbed by the package turns to steam and expands rapidly. The stress caused by this expanding moisture results in internal and external cracking of the package that leads to reliability failures. Possible damage includes the delamination of the plastic from the chip surface and lead frame, damaged bonds, cratering beneath the bonds, and external package cracks.

To prevent potential damage, packages that are susceptible to the effects of moisture expansion undergo a process called dry pack. This dry-pack process helps reduce moisture levels inside the package. The process consists of a 24-hour bake at 125°C followed by sealing of the packages in moisture-barrier bags with desiccant to prevent reabsorption of moisture during the shipping and storage processes. These moisture-barrier bags allow a shelf storage of one year from the date of seal at < 40°C and < 90% relative humidity. Once the moisture-barrier bag is opened, the devices in it must be handled by one of the following four methods, listed in descending order of preference:

- The devices may be mounted within x hours (see Table 3), depending on the moisture-sensitivity level of the package (see Table 4) in an atmospheric environment of less than 60% relative humidity and less than 30°C.
- The devices may be stored outside the moisture-barrier bag in a dry-atmospheric environment of less than 20% relative humidity until future use.
- The devices may be resealed in the moisture-barrier bag adding new fresh desiccant to the bag. When the bag is opened again, the devices should be used within the x-hour time limit or resealed again with fresh desiccant.
- The devices may be resealed in the moisture-barrier bag using the original desiccant. This method does not allow the floor life of the devices to be extended. The cumulative exposure time before reflow must not exceed a total of x hours.

Plastic surface-mount FIFO devices are tested for moisture sensitivity in accordance with JESD A112-A, “Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices” and IPC SM-786A, “Procedures for Characterizing and Handling of Moisture/Reflow-Sensitive IC’s.”

Table 3. Exposure Time Versus Moisture-Level Classification

MOISTURE LEVEL	X HOURS
2	8,760 (1 year)
3	168
4	72
5	48
6	6

Packing Methods/Quantities/Moisture Sensitivity/Dry Pack

TI uses three kinds of packing to ship FIFOs to customers: tubes, tape/reel, and trays. The quantities for each kind of packing are listed in Table 4. The shipping quantity is defined as the maximum number of packages that can be packed in a single shipping unit (e.g., the maximum number of 56-pin SSOP packages that can be packed in a tube is 20). Whether or not the packages require dry pack before shipping is noted in the dry-pack column.

Table 4. Packing Methods and Quantities

PACKAGE†	PACKING METHOD			MOISTURE SENSITIVITY LEVEL	DRY PACK
	TUBE‡	TAPE/REEL‡	TRAYS‡		
24-pin SOIC (DW)	25	1000	N/A	1	No
28-pin SOIC (DW)	20	1000	N/A	1	No
44-pin PLCC (FN)	26	500	N/A	1	No
56-pin SSOP (DL)	20	1000	N/A	1	No
64-pin TQFP (PM)	N/A	N/A	160	4	Yes
64-pin TQFP (PAG)	N/A	N/A	160	2	Yes
68-pin PLCC (FN)	18	250	N/A	2	Yes
80-pin TQFP (PN)	N/A	N/A	96	2	Yes
80-pin PQFP (PH)	N/A	N/A	66	3	Yes
120-pin TQFP (PCB)	N/A	N/A	24	2	Yes
132-pin PQFP (PQ)	N/A	N/A	36	3	Yes

† (xx) = TI package nomenclature
‡ TI reserves the right to change any of the shipping quantities at any time without notice.
N/A = not applicable

Package Dimensions and Area Comparison

Figure 1 contains two-dimensional drawings of the ten available surface-mount FIFO packages. The dimensions given are averages. For detailed mechanical drawings of these packages, please refer to the mechanical drawing section of the 1996 *High-Performance FIFO Memories Data Book*, literature number SCAD003C.

Figure 2 shows the area comparison of surface-mount packages for FIFOs from TI and other FIFO vendors.

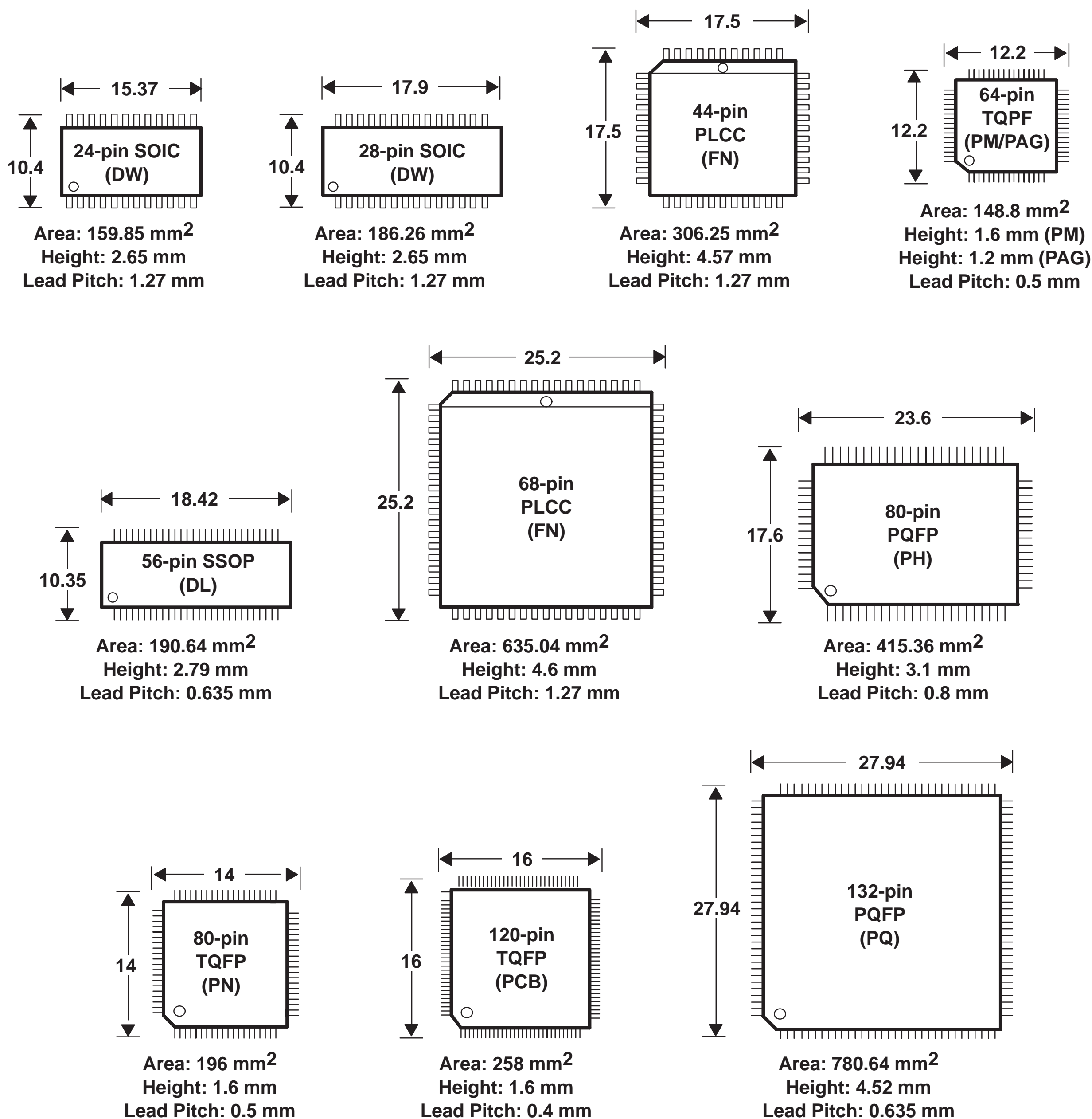

Figure 1. Package Dimensions

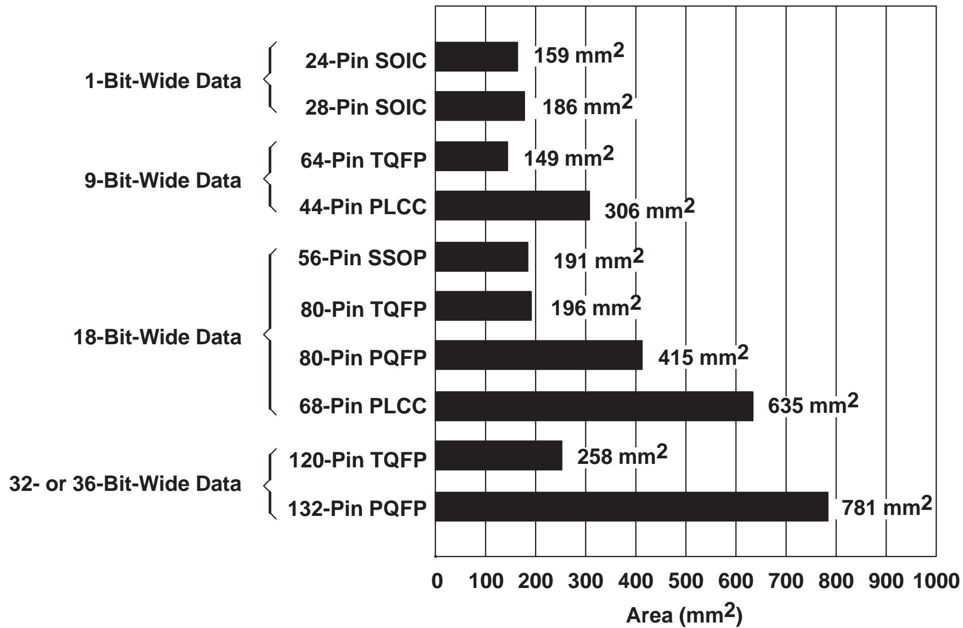

Figure 2. Surface-Mount Package Area Comparison

Test Sockets

For prototype development of a system, it is often an advantage to have sockets for surface-mount products. Test sockets available for use with TI FIFO packages are listed in Table 5. Only one manufacturer is listed for each socket type, although other vendors may offer comparable sockets.

Table 5. Test Sockets for FIFO Packages

PACKAGE	MANUFACTURER	NUMBER	DESCRIPTION
24-pin SOIC (DW)	Enplas	FP-24-1.27-08	N/A
28-pin SOIC (DW)	Enplas	FP-28-1.27-06	N/A
44-pin PLCC (FN)	NEY	6044	Solder through hole
56-pin SSOP (DL)	Yamaichi	IC51-0562-1387	Solder through hole
64-pin TQFP (PM or PAG)	Yamaichi	IC51-0644-807	Solder through hole
68-pin PLCC (FN)	Yamaichi	IC51-0684-390	Solder through hole
80-pin PQFP (PH)	Yamaichi	IC51-0804-394	Solder through hole
80-pin TQFP (PN)	Yamaichi	IC51-0804-808	Solder through hole
120-pin TQFP (PCB)	Yamaichi	IC51-1204-1596	Solder through hole
132-pin PQFP (PQ)	Yamaichi	IC51-1324-828	Solder through hole

Acknowledgment

The authors of this document are Tom Jackson and Mary Helmick. Revisions were made by Bill Manson and Thomas Lewis (February 1997).